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VHDL TECHNOLOGY LIBRARY METHOD FOR EFFICIENT CUSTOMIZATION OF CHIP GATE DELAYS

Abstract of the Disclosure

A method and system update a VHDL technology library (306) to incorporate correlated delay values by reading the VHDL technology library (306), inserting a tpd_super_rise_time generic declaration and a tpd_super_fall_time generic declaration for every VHDL gate model in the VHDL technology library (306), initializing other generic variables in every VHDL gate model in the VHDL technology library to an equation representing a correlation policy; and outputting an updated VHDL technology library. Then, the method and system bind correlated delay constants in a 3-dimensional variable data array structure to a VHDL technology library (306) using a VHDL package embedded with the correlation delay data.

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